

# Intel<sup>®</sup> Dialogic<sup>®</sup> D/41JCT-LS Four-Port Analog Converged Communications Board

The D/41JCT-LS is a four-port analog converged communications board used for developing global enterprise applications such as unified messaging, IVR and contact centers. The D/41JCT-LS supports voice, fax, and software-based speech recognition processing in a single PCI slot, providing four ana-



log telephone interface circuits for direct connection to analog loop start lines.

The D/41JCT-LS board, a part of the Intel® Dialogic® PCI product family, conforms to the H.100 CT Bus standard. The open architecture enables developers to build converged

#### **Features and Benefits**

Supports continuous speech processing, a flexible speech processing technology that couples with efficient drivers to offload critical real-time signal processing in speech-enabled applications to onboard DSPs. This reduces system latency, increases recognition accuracy, and improves overall system response time for high-density speech solutions.

Universal 32-bit PCI edge-connector for compatibility with 3.3 volt and 5.0 volt bus signals. This enables deployment in a wide variety of PCI chassis from popular manufacturers.

Configure multiple boards in a single chassis, PCI bus, or mixed PCI/ISA bus, for easy and cost-effective system expansion up to 32 analog ports.

Intel® Dialogic® Spring Ware firmware, downloadable signal and call processing firmware, provides field-proven performance based on over three million installed ports with access to future feature enhancements.

PerfectDigit DTMF (touchtone) provides reliable detection during voice playback. It lets callers "type-ahead" through menus.

A-law or  $\mu$ -law voice coding at dynamically selectable data rates, 24 Kb/s to 64 Kb/s, selectable on a channel-by-channel basis for optimal tradeoff between disk storage and voice quality.

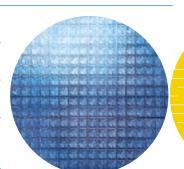
International Caller ID capability via on-hook audio path. Supports Bellcore CLASS, UK CLI, Japanese Caller ID, and other international protocols.

Intel® NetMerge $^{\text{TM}}$  Converged Communications Server Software support facilitates multi-application development.

Patented outbound call progress analysis monitors outgoing call status quickly and accurately.

Software development kits (SDKs) for Windows NT\*/Windows 2000\*, and Linux\* operating systems yield faster time to market.

Optional onboard global dial pulse detection (global DPD) feature enables callers with non-touchtone phones to access applications without additional "pulse-to-tone conversion" equipment.



# Intel in Communications

communications solutions using products from multiple vendors. And since you can install multiple D/41JCT-LS boards in a single PC chassis, you can build systems scaling up to 32 ports.

Downloaded Spring Ware firmware algorithms, executed by the onboard DSP, provide variable voice coding at 24 and 32 Kb/s ADPCM, and 48 and 64 Kb/s μ-law or A-law PCM, as well as μ-law to A-law conversion. Sampling rates and coding methods are selectable on a channel-by-channel basis. Applications can dynamically switch sampling rate and coding method to optimize data storage or voice quality as the need arises. Additional coding algorithms (such as GSM and G.726) are available for use in applications that support the Voice Profile for Internet Mail (VPIM) standard.

Spring Ware firmware also provides reliable DTMF detection, DTMF cut-through, and talk off/play off suppression over a wide variety of telephone line conditions.

Global dial pulse detection (global DPD) algorithm, available as a software option for the D/41JCT-LS board, lets you use the board in countries with limited touchtone telephone service. The Global DPD product can be optimized on a country-by-country basis to provide superior dial pulse detection.

Intel voice products offer a rich set of advanced features, including state-of-the-art DSP technology and signal processing algorithms, for building the core of any converged communications system. With industrystandard PCI bus expansion boards, you can easily and cost effectively integrate Intel voice products into exactly the type of system you need, enjoying superior performance.

### **Configurations**

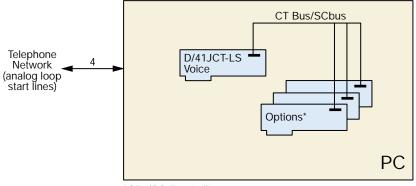
Use the D/41JCT-LS board to build sophisticated CT systems with capabilities such as speech recognition, facsimile, and text-to-speech (TTS). The D/41JCT-LS board shares a common hardware and firmware architecture with other Intel CT Bus and SCbus-based boards for maximum flexibility and scalability. Add features or grow the system while protecting your investment in hardware and application code. Applications can be easily ported to lower- or higher-line-density platforms with only minimum modifications.

The D/41JCT-LS board installs in any PCI-based PC or server (PCI bus or mixed PCI/ISA) and compatible computers (Intel 386™, Intel 486™, or Pentium® processor-based PC platforms). The D/41JCT-LS board provides everything required for building integrated voice solutions scalable from 4 ports to 32 ports. The maximum number of lines that can be supported depends on the application, the amount of disk I/O required, and the host computer CPU and power supply.

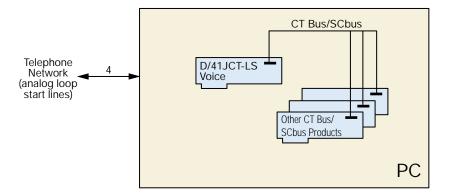
The D/41JCT-LS board can operate within a mixed chassis containing Intel PCI and ISA products. The forward-looking design of the D/41JCT-LS conforms to the new H.100 CT Bus to enable connection to nextgeneration CT Bus products. The D/41JCT-LS can also connect to existing SCbus products through the use of an optional CT Bus/SCbus adapter. The adapter provides both SCbus and H.100 physical connectors required to link the D/41JCT-LS to current SCbus products.

#### **Applications**

- Voice mail/messaging
- Interactive voice response
- Contact center
- Audiotex
- Operator services
- Dictation
- Auto dialers
- Unified messaging
- Online data entry/query

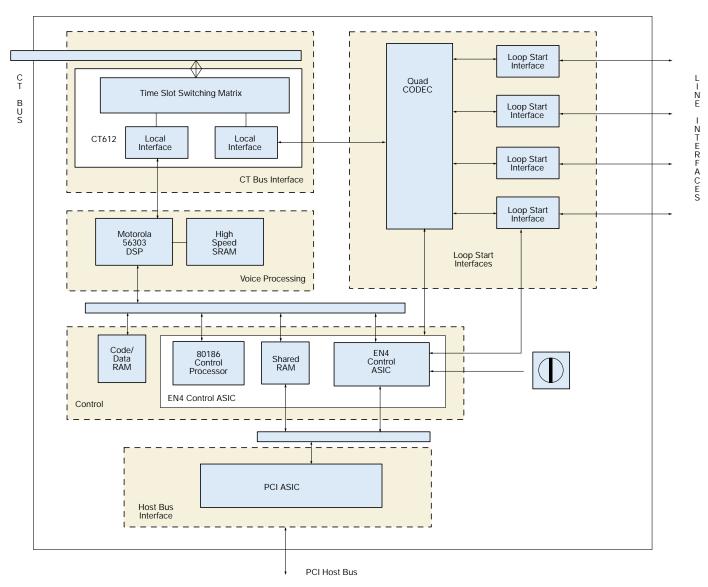


- \*CP6/SC Facsimilie
- \*Antares™ DSP Platforms
- \*Other third-party SCbus resources



## **Software Support**

The D/41JCT-LS board is currently supported by the Intel® Dialogic® System Release (SR) software and software development kits (SDKs) for Windows NT and Windows 2000, and the SR software and SDKs for Linux operating systems. These packages contain a set of tools for developing complex multichannel applications.



**Functional Block Diagram** 

## **Functional Description**

The D/41JCT-LS board uses a unique dual-processor architecture that combines the signal processing capabilities of a DSP with the decision-making and data movement functionality of a general-purpose 80186 control microprocessor. This dual-processor approach off-loads many low-level decision-making tasks from the host computer and thus enables easier development of more powerful applications. This architecture handles real-time events, manages data flow to the host PC for faster system response time, reduces host PC processing demands, processes DTMF and telephony signaling, and frees the DSP to perform signal processing on the incoming call.

Each of four analog loop start telephone line interfaces on the D/41JCT-LS board receives analog voice and telephony signaling information from the telephone network (see block diagram). Each telephone line interface uses reliable, solid-state hook switches (no mechanical contacts) and FCC-part 68 class B ring detection circuitry. This FCC-approved ring detector is less susceptible to spurious rings created by random voltage fluctuations on the network. Each interface also incorporates circuitry that protects against high-voltage spikes and adverse network conditions and lets applications go off-hook any time during ring cadence without damaging the board.

Inbound telephony signaling (ring detection, loopcurrent detection, and Caller ID information) is

detected by the line interface and routed via a control bus to the control processor. The control processor responds to these signals, informs the application of telephony signaling status, and instructs the line interface to transmit outbound signaling (on-hook/off-hook) to the telephone network.

Based on Spring Ware firmware loaded in DSP RAM, the DSP performs the following signal analysis and operations on this incoming data:

- Automatic gain control to compensate for variations in the level of the incoming audio signal
- Applies an ADPCM (Adaptive Differential Pulse Code Modulation) or PCM (Pulse Code Modulation) algorithm to compress the digitized voice and save disk storage space
- Detects the presence of tones DTMF, MF, or an application-defined single or dual tone
- Silence detection to determine whether the line is quiet and the caller is not responding

For outbound data, the DSP performs the following operations:

- Expands stored, compressed audio data for playback
- Adjusts the volume and rate of speed of playback upon application or user request
- Generates tones DTMF, MF, or any applicationdefined general-purpose tone

The dual-processor combination also performs the following outbound dialing and call progress monitoring:

- Transmits an off-hook signal to the telephone network
- Dials out (places an outbound call)
- Monitors and reports results: line busy or congested; operator intercept; ring, no answer; or if the call is answered, whether answered by a person, an answering machine, a facsimile machine or a modem

The D/41JCT-LS board also supports optional Global DPD software that recognizes dial pulse digits even in the most difficult telephony environments.

When recording speech, the DSP can use different digitizing rates from 24 to 64 Kb/s as selected by the application for the best speech quality and most efficient storage. The digitizing rate is selected on a channel-by-channel basis and can be changed each

time a record or play function is initiated. The DSP processed speech is transmitted via the control processor to the host PC for disk storage. When replaying a stored file, the processor retrieves the voice information from the host PC and passes it to the DSP, which converts the file into digitized voice. The DSP sends digitized voice and appropriate signaling responses to the codec to be converted into analog format for transmission to the telephone network.

Signaling data (on-/off-hook, ringing, Caller ID, etc.) is passed to the onboard control processor and transmitted to the application via a dual-port shared RAM and the host PCI bus.

When using the D/41JCT-LS board and the CT Bus, digital voice and signaling information from a network board or other resource enter the board via the H.100 connector and CT Bus interface. A CT612 chip manages these signals and acts as the traffic coordinator and matrix switch to buffer the high-speed digital data from the bus until the data for each channel can be transmitted to the DSP.

The CT612 chip transmits several lower speed data streams over the CT Bus high-speed channel. The bus configuration is set when the firmware is downloaded at system initialization. This chip incorporates matrix switching capabilities. Under control of the onboard control processor, the CT612 chip can connect any call being processed to any of the four analog lines or to any of the 4096 CT Bus time slots. This enables the application to switch calls to or from other resources. such as facsimile or speech recognition, as they are needed, or to reroute calls.

The onboard control processor controls all operations of the D/41JCT-LS board via a local bus and interprets and executes commands from the host PC. The processor handles real-time events, manages data flow to the host PC to provide faster system response time, reduces PC host processing demands, processes DTMF and telephony signaling before passing them to the application, and frees the DSP to perform signal processing.

Communications between a processor and the host PC is via the Shared RAM that acts as an input/output buffer and thus increases the efficiency of disk file transfers. This RAM interfaces to the host PC via the PCI bus. All operations are interrupt-driven to meet the demands of real-time systems. When the system is

**Datasheet** Intel® Dialogic® D/41JCT-LS Four-Port Analog Converged Communications Board

initialized, Spring Ware firmware is downloaded from the host PC to the onboard code/data RAM and DSP RAM to control all board operations. This downloadable firmware gives the board all of its intelligence and enables easy feature enhancement and upgrades.

With the rotary switch on the D/41JCT-LS board set to 0, the D/41JCT-LS board is plug-and-play enabled.

Configuration is handled exclusively by software. Alternatively, you can set the rotary switch to another value to manually control board location for ease of cabling or backwards compatibility with Intel® Dialogic® Board Locator Technology (BLT) installation.

## Technical Specifications\*

Technical Specifications*		
	Number of ports	4
	Maximum boards/system	8
	Analog network interface	On-board loop start interface circuits
	Resource sharing bus	CT Bus, SCbus compatible with bus adapter
	Control processor	80C186 @ 34.8 MHz
	Digital signal processor	Motorola* DSP56303 @100 MHz, with 128Kx24 private SRAM
Host Interface		
	Bus compatibility	PCI (complies with PCISIG Bus Specification, Rev. 2.1)
	Bus speed	33 MHz maximum
	Bus mode	Target mode operation only
	Shared memory	32 KB page
	I/O ports	None
Telephone Interfac	ce <sup>†</sup>	
	Trunk type	Loop start
	Loop current range	20 mA to 120 mA
	Impedance	600 Ohms nominal
	Ring detection	15 Vrms min., 13 Hz to 68 Hz, (configurable by parameter)
	Echo return loss	Configurable by software parameter
	Crosstalk coupling	Less than -70 dB at 1 KHz channel to channel
	Receive signal/noise ratio	70 dB referenced to -15 dBm
	Frequency response	200 Hz to 3400 Hz ±3 dB (transmit and receive)
	Connector	Four RJ-11 type
Environmental Re	quirements	
	+5 VDC	750 mA max.
	+12 VDC	200 mA max.
	–12 VDC	100 mA max.
	Operating temperature	0°C to +50°C
	Storage temperature	-20°C to +70°C
	Humidity	8 to 80% noncondensing
	Form factor	Universal slot (5 V or 3.3 V) PCI long card, 12.3 in. long (without edge retainer) or 13.3 in. long (with edge retainer), 0.79 in. wide (total envelope), 3.87 in. high (excluding edge connector)
Safety and EMI Co	ertifications	
	United States	FCC Part 15 class A FCC Part 68 EBZUSA-75385-VM-T UL: E96804 UL1950
	Canada	DOC: 885-5542A
		For specific country approval designation, see the Intel Communications Systems Products Global Product Approvals listing on the Intel Web site or contact your Intel Technical Sales Representative
	Estimated MTBF	274,000 hours per Bellcore* Method <sup>1</sup>
	Warranty	
	North America	Three years for purchases made directly from Intel. For purchas es not made directly from Intel, please contact your vendor regarding the warranty period offered by such vendor.
	Outside North America	Contact your nearest regional office for warranty information.

<sup>&</sup>lt;sup>†</sup> Analog levels: 0 dBm0 corresponds to a level of +3 dBm at tip-ring analog point. Values vary depending on country requirements; contact your account manager. <sup>‡</sup> Average speech mandates +16 dB peaks above average and preserves -13 dB valleys below average.

Facsimilie		
. 403	Fax compatibility	ITU-T G3 compliant (T.4, T.30) ETSI NET/30 compliant
	Data rate	14,400 b/s (v.17) send 9600 b/s receive
	Variable speed selection	Automatic step-down to 12,000 b/s, 9600 b/s, 7200 b/s, 4800 b/s, and lower
	Transmit data modes	Modified Huffman (MH)
	Modified Read (MR)	
	Receive data modes	MH, MR
	File data formats	Tagged Image File Format (TIFF/F) for transmit/receive MH and MR
	ASCII-to-fax conversion	Host-PC-based conversion Direct transmission of text files All Windows fonts supported Page headers generated automatically
	Error correction	Detection, reporting, and correction of faulty scan lines
	Image widths	215 mm (8.5 in.) 255 mm (10.0 in.) 303 mm (11.9 in.)
	Image scaling	Automatic horizontal and vertical scaling between page sizes
	Polling modes	Normal Turnaround
	Image resolution	Normal (203 pels/in. x 98 lines/in.) Fine (203 pels/in. x 196 lines/in.)
	Fill minimization	Automatic fill bit insertion and stripping
Audio Signal		
rtualo olgilal	Receive range	-40 dBm to +2.5 dBm0 nominal, configurable by parameter
	Automatic gain control	Application can enable/disable. Above –18 dBm0 results in full-scale recording, configurable by parameter.
	Silence detection	-40 dBm nominal, software adjustable <sup>↑</sup>
	Transmit level (weighted average)	-9.5 dBm0 nominal, configurable by parameter <sup>†</sup>
	Transmit volume control	40 dB adjustment range, with application-definable increments and legal limit cap
Frequency Response		
. , ,	24 Kb/s	300 Hz to 2600 Hz ±3 Db
	32 Kb/s	300 Hz to 3400 Hz ±3 dB
	48 Kb/s	300 Hz to 2600 Hz ±3 dB
	64 Kb/s	300 Hz to 3400 Hz ±3 dB
Audio Digitizing		
· ···· - · · · · · · · · · · · · · · ·	13 Kb/s	GSM @ 8 kHz sampling
	24 Kb/s	OKI® ADPCM @ 6 kHz sampling
	32 Kb/s	OKI® ADPCM @ 8 kHz sampling
	32 Kb/s	G.726 @ 8 kHz sampling
	48 Kb/s	μ-law PCM @ 6 kHz sampling
	64 Kb/s	μ-law PCM @ 8 kHz sampling
	Digitization selection	Selectable by application on function call-by-call basis
	Playback speed control	Pitch controlled Available for 24 and 32 Kb/s data rates Adjustment range: ±50% Adjustable through application or programmable DTMF control

#### Spring Ware Firmware Technical Specifications (cont.)

#### **DTMF Tone Detection**

DTMF digits 0 to 9, \*, #, A, B, C, D per Bellcore LSSGR Sec 6

-38 dBm to +3 dBm per tone, configurable by parameter† Dynamic range Minimum tone duration 40 ms, can be increased with software configuration

Interdigit timing Detects like digits with a >40 ms interdigit delay

Detects different digits with a 0 ms interdigit delay

Twist and frequency variation Meets Bellcore LSSGR Sec 6 and EIA 464 requirements

Noise tolerance Meets Bellcore LSSGR Sec 6 and EIA 464 requirements for Gaussian,

impulse, and power line noise tolerance

Cut-through Local echo cancellation permits 100% detection with a >4.5 dB return loss

Talk off Detects less than 20 digits while monitoring Bellcore TR-TSY-000763

standard speech tapes (LSSGR requirements specify detecting no more than 470 total digits). Detects 0 digits while monitoring MITEL speech tape

#CM 7291.

Global Tone Detection

Programmable for single or dual Tone type

Max. number of tones Application-dependent

Programmable within 300 Hz to 3500 Hz Frequency range Max. frequency deviation Programmable in 5 Hz increments

Frequency resolution ± 5 Hz. Separation of dual-frequency tones is limited to 62.5 Hz at a

signal-to-noise ratio of 20 dB.

Timing Programmable cadence qualifier, in 10 ms increments Programmable, default set at -6 dBm0 to +3 dBm0 per tone Dynamic range

Global Tone Generation

Tone type Generate single or dual tones

Frequency range Programmable within 200 Hz to 4000 Hz

Frequency resolution 1 Hz

Duration 10 ms increments

**Amplitude** -43 dBm0 to -3 dBmo per tone, programmable

MF Signaling

MF digits 0 to 9, KP, ST, ST1, ST2, ST3 per Bellcore LSSGR Sec 6, TR-NWT-000506

and CCITT Q.321

Transmit level Complies with Bellcore LSSGR Sec 6, TR-NWT-000506 Signaling mechanism Complies with Bellcore LSSGR Sec 6, TR-NWT-000506

Dynamic range for detection -25 dBm0 to +3 dBm0 per tone

Acceptable twist 6 dB

Acceptable frequency variation Less than ±1 Hz

# Spring Ware Firmware Technical Specifications (cont.)

Call Progress Aanalysis		
- ,	Busy tone detection	Default setting designed to detect 74 out of 76 unique busy/congestion tones used in 97 countries as specified by CCITT Rec. E., Suppl. #2. Default uses both frequency and cadence detection. Application can select frequency only for faster detection in specific environments.
	Ring back detection	Default setting designed to detect 83 out of 87 unique ring back tones used in 96 countries as specified by CCITT Rec. E., Suppl. #2. Uses both frequency and cadence detection.
	Positive voice detection accuracy	>99% based on tests on a database of real world calls in North America. Performance in other markets may vary.
	Positive voice detection speed	Detects voice in as little as 1/10th of a second
	Positive answering machine detection accuracy	>85% based on application and environment
	Fax/modem detection	Pre-programmed
	Intercept detection	Detects entire sequence of the North American tri-tone. Other intercept tones sequences can be programmed.
	Dial tone detection before dialing	Application enable/disable Supports up to three different user-definable dial tones Programmable dial tone drop out debouncing
Tone Dialing		0 to 9, *, #, A, B, C, D per Bellcore LSSGR Sec 6, TR-NWT-000506
	DTMF digits	
	Frequency variation	Less than ±1 Hz
	Rate	10 digits/s maximum, configurable by parameter <sup>†</sup>
	Level	-4.0 dBm0 per tone, nominal, configurable by parameter <sup>†</sup>
Pulse Dialing		
	10 digits	0 to 9
	Pulsing rate	10 pulses/s, nominal 20 pulses/s for Japan, configurable by parameter <sup>†</sup>
	Break ratio	60% nominal, configurable by parameter <sup>†</sup>
Analog Caller Identificat	ion	
3	Applicable standards	Bellcore TR-TSY-000030 Bellcore TR-TSY-000031
		TAS T5 PSTN1 ACLIP: 1994 (Singapore)
	Modem standard	Bell 202 or V.23, serial 1200 bits/sec (simplex FSK signaling)
	Receive sensitivity	-48 dBm (-50 dBv) to -1 dBm
	Noise tolerance	Minimum 18 dB SNR over 0 to -48 dBm dynamic range for error-free performance $$
	Data formats	Single Data Message (SDM) and Multiple Data Message (MDM) formats via API calls and commands
	Line impedance	AC coupled 600 Ohm (@ 1.8 kHz) termination during Caller ID on-hook detection interval
	Message formats	ASCII or binary SDM, MDM message content
Analog Display Services	Interface (ADSI)	
. J . I		FSK generation per Bellcore TR-NWT-000030
		CAS tone generation and DTMF detection per Bellcore TR-NWT-001273.

<sup>&</sup>lt;sup>1</sup> Analog levels: 0 dBm0 corresponds to a level of +3 dBm at tip-ring analog point. Values vary depending on country requirements; contact your account manager.

<sup>1</sup> Average speech mandates +16 dB peaks above average and preserves -13 dB valleys below average.

#### **Hardware System Requirements**

- Intel 386<sup>™</sup>, Intel 486<sup>™</sup>, or Pentium® microprocessor PCI bus or mixed PCI/ISA bus computer
- Operating system hardware requirements vary according to the number of channels being used.
- System must comply with PCISIG Bus Specification Rev. 2.1 or later.

### **Additional Components**

- Multidrop CT Bus cables (CBLCTB68C3DROP, CBLCTB68C4DROP, CBLCTB68C8DROP, CBLCTB68C12DROP, CBLCTB68C16DROP)
- CT Bus/SCbus adapter (CTBUSTOSCBUSADP)
- SCbus terminator kits (1SCBUS1TERMKIT, 2SCBUS1TERMKIT, 3SCBUS1TERMKIT)

To learn more, visit our site on the World Wide Web at www.intel.com

1515 Route Ten Parsippany, NJ 07054 Phone: 1-973-993-3000 Fax: 1-973-993-3093

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